REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated May 18, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-5 are under consideration in this application. Claims 1 and 4 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention. Claims 6-7 are being cancelled without prejudice or disclaimer.

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Informality Rejections

Claim 6 was rejected under 35 U.S.C. § 112, first paragraph, as not being enabled by the specification, and claim 7 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

As claims 6-7 are being cancelled without prejudice or disclaimer, the rejections thus become moot.

Prior Art Discussion

Claims 1 - 5 remain rejected under 35 U.S.C. §102(e) on the grounds of being anticipated by US Pat. No. 6,678,645 to Rajsuman et al. (hereinafter "Rajsuman"). This rejection has been carefully considered, but is most respectfully traversed as follows.

The semiconductor integrated circuit device 60 of the invention, as now recited in claim 1 (e.g., Fig. 1), comprises: first and second circuit blocks 601, 602; an interface checker 70 integrated into the semiconductor integrated circuit device as one simulation model ("*Into the semiconductor integrated circuit chip 60, an interface checker 70 for design data A is*

also integrated" p. 7, lines 20-22; "*The above interface checker 70 for design data A is composed of logic circuits incorporated into the semiconductor integrated circuit chip 60.*" P. 8, lines 15-17; "*This hardware description, testbench description stored in a storage unit 100, design data A stored in a storage unit 50, and design data B stored in a storage unit 90 are input to a logic simulator/emulator model, and then this model can execute logic simulation. ... the interface checker can be incorporated into a run model for logic emulator and high-speed logic verification can be performed*" p. 11, lines 5-22) and monitors whether waveforms of signals between the first and second circuit blocks 601, 602 conform to an interface specification of a design data of the first circuit block 601; and an external output pin 80 which outputs outside of the semiconductor integrated circuit device 60 a result of a monitoring of the interface checker.

The invention as recited in claim 4 is directed to a design method of a semiconductor integrated circuit device 60 comprising: providing a design data and an interface specification of the design data; generating a synthesizable interface checker in accordance with the interface specification; producing a semiconductor integrated circuit device 60 including a first circuit block 601 according to the design data and the interface checker 70 according to the synthesizable interface checker; and using the interface checker 70 integrated into the semiconductor integrated circuit device 60 as one simulation model to monitor whether waveforms of signals between the first circuit block 601 and another circuit block 602 conform to the interface specification of the design data.

"Because the interface checker has conventionally taken the simulation efficiency as important and ignored logic synthesis capability, it has been impossible to use the interface checker for a run model for a logic emulator that is specialized hardware. In the present invention, because the hardware description of the synthesizable interface checker can be synthesized, the interface checker can be incorporated into a run model for logic emulator and high-speed logic verification can be performed (p. 11, lines 18-22)."

As such, the invention not only incorporates the interface checker 70 into the semiconductor integrated circuit device 60 for logic synthesis and verification during the design stage, but also integrates the interface checker 70 into the semiconductor integrated circuit device 60 as one simulation model to monitor waveforms conformation after the semiconductor integrated circuit device 60 is fabricated ("*an object of the present invention is to provide means for determining whether any functional block included in a system LSI has*

a design error or is used by incorrect usage in the event that the system LSI malfunctions after fabricated" p. 4, lines 22-26)

Applicants respectfully contend that Rajsuman fails to teach or suggest such an "interface checker 70 integrated into a semiconductor integrated circuit device 60 as one simulation model for logic synthesis and verification during the design stage, and to monitor waveforms conformation after the semiconductor integrated circuit device 60 is fabricated (during the actual use of the semiconductor device)" or "an external output pin outputting outsides of the semiconductor device a result from the interface checker" according to the invention.

Contrary to the Examiner's assertion (p. 5, 2nd paragraph of the outstanding Office Action) that "the limitation of an interface checker that is part of or installed on the semiconductor device is already disclosed by Rajsuman (col., lines 52-65)", Applicants respectfully contend that Rajsuman never disclose that its cores A-E or it verification units (VU) 661- 685 (arguably corresponding to the interface checker 70 of the invention) are integrated into a SoC integrated in ONE chip as one simulation model. In contrast, Rajsuman's cores A-E (software) are formulated in the separated silicon ICs 661- 685, rather than any actual cores (hardware) integrated into ONE chip as one simulation model, to be verified on VUs 661- 665 (col. 10, lines 46-48).

In addition, Rajsuman's verification units (VU) 661- 685 in the design validation stations DVS1-DVS5 merely apply test patterns produced based on the testbench data to the corresponding silicon IC/core (col. 8, lines 13-15) in a standing-alone manner, rather than being integrated into the SoC as one simulation model as the interface checker 70 of the invention.

"*Rather than directly testing the complete SoC, separate ICs representing individual cores in the SoC 43, such as cores A, B and C are utilized in the design validation station 50* (col. 6, last line – col. 7, lines)." Rajsuman (Fig. 5) then verifies each of the cores by placing individual cores 681-685 on design validation stations DVSs 50 and using an interconnect bus 71 of to transact the data between the individual cores (col. 10, line 52 - col. 11 line 3).

In other words, Rajsuman only has ***external*** validation stations for testing each of the blocks/cores of the SoC, but not any interface checker integrated into the semiconductor integrated circuit device SoC as one simulation model to monitor waveforms conformation of the whole SoC.

Second, the interface of each of Rajsuman's blocks/cores can only be physically verified by transactions anticipated during the test, rather than after the SoC is fabricated and in the actual usage as the invention (p. 4, lines 21-26). Rajsuman can only verify each core "*to be integrated in the SoC* (Abstract, line 4)", but not after the SoC is fabricated.

Applicants contend that the cited prior art reference fails to teach or disclose each and every feature of the present invention as recited in independent claims 1 and 4. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference. Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

September 19, 2005

SPF/JCM/JT